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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,632	11/13/2000	Alexander L. Minkin	019680-00200US	3726

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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
QUILLEN, ALLEN E	
ART UNIT	**PAPER NUMBER**
2676	4

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/712,632	MINKIN	
	Examiner	Art Unit	
	Allen E. Quillen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-14 and 33-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-14 and 33-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Claims 1-9, 15-32 are cancelled; claims 33-60 added. All claims are pending. Specification change to show related application data and the formal drawings are received and acknowledged. Applicant's arguments filed May 28, 2003 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 10-14, 33-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook, et al, U.S. Patent 6,353,438.

4. Regarding claim 10, representative of claims 57, and 11-14, 55-56, 58-60, Van Hook discloses a method of storing a texel in a texel cache (Figures 1A, 1B, 1C; Figure 9; Columns 2, lines 9, 20-27, 40-44, 55 through Column 2, line 47; Column 8, lines 20-21; Column 10, lines 8 through Column 11, line 5) comprising: reading (*transferring, requests, texture mapping, texel address information in S and T coordinates, pixels,* Column 10, lines 12, 26-34) a t coordinate of the texel, the t coordinate comprising a plurality of bits; reading a s coordinate of the texel, the s coordinate comprising a plurality of bits; and forming an offset (*memory mapping;* Column 11, lines 1-5; 36-47) by concatenating bits of the t coordinate with bits of the s coordinate (*...the "resolution" of the pixel is the size of the number value used to describe each pixel. The size of the number value is limited by the number of "bits" in the memory available to describe each pixel...one bit...two bits..32-bit...the number of bits...,* Column 1, lines 45-60; Column 2, lines 20-27; Figures 7 and 8, *tiled caching, address location where the image data (i.e., texels) begins in DRAM...Tile 0 comprises a tile location at S and T coordinates (S_0, T_0) with respect to base address...Each tile comprises a two-dimensional array of texels..., tiles=> texels=> bytes=> bits,* Column 9, lines 16-29, 40-56; Column 10, lines 49- 57;Column 12, lines 5-9; Column 12, lines 57-58, 61-67; *non-contiguous storage locations,* Column 8, line 64 through Column 9, line1-5; *direct mapped, two-way associative, set associative,* Column 13, lines 12-16, *..the tag index is comprised of the middle bits of the texel,* lines 46-47, *Bits 0-5,* line 51, *middle bits,* lines 60-61, *middle bits,* line 65; Column 14, lines 1-7, *upper bits,* lines 64-66), wherein the texel is associated with a MIPmap having a level of detail (Figure 12, Column 7, lines 28-48; Column 15, lines 58-59; Column 16, lines 38 through Column 17, line 17) comprising a plurality of bits, further comprising forming an index signal (Column 7, lines 20-34; 42-47, *an index assigned to*

a specific cache line. ....tag information identifies the tile..) by concatenating middle order bits of the s coordinate, middle level bits of the t coordinate, and at least one bit of the level of detail (Figures 7-9, 11-12, *resolution, trilinear MIP-mapping,* see *pixel values* above; Column 4, lines 8-47);

[Claims 11 and 58] texture identification (see above, Column 7, line 27, *tag information identifies*) at least one bit of the texture identification (see *bits* above);

[Claims 12 and 59] r coordinate (see above; [Examiner interprets that the r coordinate is used in 3D texturing applications using a r, s and t coordinate system, as Van Hook discloses: *3D, trilinear mipmapping...filtering, RGB, depth cueing*, Column 2, lines 35-54; Column 15, lines 8-11; 34-35) at least one bit of the r coordinate (see *bits* above);

[Claim 13 and 60] a main memory address (Figures 7-9, see above, DRAM, Column 7, lines 23-25), at least one bit of the main memory address (see *bits* above).

[Claim 14 and 56] An integrated circuit (Figures 10A, element 1030; 10B; Column 17, lines 50-54) comprising: a texture cache subsystem for storing a texel (Figure 9, element 901); a cache address generator subsystem configured to provide an index and offset to the texture cache subsystem (903); and a graphics pipeline subsystem configured to provide an s coordinate, a t coordinate, and a memory address to the cache address generator subsystem (904), and further configured to receive the texel from the texture cache subsystem, wherein the index comprises bits of the s and t coordinates and at least on bit selected from the group consisting of level of detail, a texture id, a memory address, and an r coordinate (see above); furthermore [Claim 56], a FIFO (Column 6, line 35))coupled to receive packets of data (Figures 10A and 10B, element

1025, Column 19, lines 1-5, see above), from the texture cache manager, where the FIFO stores the packets of data for a plurality of clock cycles (Column 15, lines 1-2, 13-14, 15-25).

5. Regarding claim 33, representative of claims 38, 43, 48, Van Hook discloses the method of claim 10, wherein the forming an offset by concatenating bits of the t coordinate with bits of the s coordinate is done by concatenating the lower bits of the t coordinate with the lower order bits of the s coordinate (Column 11, lines 1-4; Column 13, lines 36-62).

6. Regarding claim 34, representative of claims 39, 44, 49, 53, Van Hook discloses the method of claim 33 further comprising storing the texel in a texel cache comprising a plurality of cache lines, wherein each cache line comprises a plurality of storage elements (see above; Column 7, line 9-11).

7. Regarding claim 35, representative of claims 40, 45, 50, 54,Van Hook discloses the method of claim 34 further comprising storing the texel in a storage element identified by the offset (see above; Column 8, line 64 through Column 9, line 5), the storage element in a cache line, the cache line identified by the index (see above; Column 7, lines 1-12, 20-50).

8. Regarding claim 36, representative of claims 41, 46, 51, Van Hook discloses the method of claim 35 further comprising retrieving the texel from a main memory, wherein the texel has an address in main memory (Column 1, line 40 through Column 2, lines 67).

9. Regarding claim 37, representative of claims 42, 47, 52, Van Hook discloses the method of claim 36 further comprising forming a tag by concatenating the high order bits of the s coordinate and high order bits of the t coordinate, adding the address in main memory, and storing the tag in a look-up table (Figure 9, Column 7, line 21).

10. Regarding claim 55, Van Hook discloses the circuit of claim 54, further comprising a memory controller coupled to the texture cache subsystem, the memory controller configured to receive and provide texels from and to an external memory (Figures 10A and 10B, elements 1030A, 1015, 1032, 1030B, 1014, Column 18, lines 11-24).

Response to Arguments

11. Applicant states, "Van Hook does not teach...at least one bit of the level of detail...on bit of texture identification...one bit of r coordinate...one bit of main memory address" (Page 10, Claim 10, lines 2-4; Page 11, line 3, Claim 12, line 4; Page 12, line 5).

12. Examiner respectfully replies, however, that in the claims, Van Hook explicitly discloses that the texel addressing is done in and at the bit level and that the features of level of detail, texture identification, r [the third label of the depth axis in a 3D] coordinate [system], main memory addressing are explicitly disclosed by Van Hook in relationship to the texel cache addressing scheme (*the number of bits...*, Column 1, lines 45-60; Column 2, lines 20-27; Figures 7 and 8, *tiled caching, address location where the image data (i.e., texels) begins in DRAM...Tile 0 comprises a tile location at S and T coordinates (S_0, T_0) with respect to base address...Each tile comprises a two-dimensional array of texels..., tiles=> texels=> bytes=> bits*, Column 9,

lines 16-29, 40-56; Figure 12, Column 7, lines 28-48; Column 15, lines 58-59; Column 16, lines 38 through Column 17, line 17; Column 7, line 27, *tag information identifies; 3D, trilinear mipmapping...filtering, RGB, depth cueing*, Column 2, lines 35-54; Column 15, lines 8-11; 34-35; Figures 7-9, see above, DRAM, Column 7, lines 23-25). Furthermore, Van Hook describes how the features described overcome the memory addressing problems: "Peak efficiency is achieved when transferring multiple data values, especially data values that are in adjacent memory locations. [but not well suited to texturing] ...burst transfer...DRAM...9 clock cycles...scan order...skips...dispersing memory operations ...[thus] the speed of the texture mapping process may be significantly reduced by the performance of DRAM data transfers with frequent address skips..." (Column 4, lines 8-37, 45-52, 64; Column 5, lines 7-12, 66-67 through Column 6, lines 1-11).

Furthermore, with respect to reducing cache thrashing, which is not in the claims, dealing with specific texels and corresponding pixels (Column 15, lines 52-57), Van Hook discloses, "To determine the neighborhood, a neighborhood operation (also referred to as a filter extent or file width) may be utilized which identifies texels that are located in close proximity (or within a predefined neighborhood of texels) of a pixel. The neighborhood operation may consist of an arithmetic or logical operation on the image sample values such as comparisons, minimums, and maximums. Further, because the neighborhood of texels are adjacent, contiguous or located in close proximity, the texels in the neighborhood can be accessed in parallel across cache memory banks and tag banks by interleaving. For example, when bilinear filtering is utilized, the four (4) texels at the odd and even texel address will be accessed which can be performed in parallel across cache memory banks (e.g., the neighboring pixels can fall in

different cache lines with the location of the cache lines interleaved across cache memory banks) and tag memory banks. Thus, since a filter operates on a contiguous multidimensional region/neighborhood, for a neighborhood of a known size, the cache tags may be organized such that all texels of the multidimensional neighborhood can reference the tag memory simultaneously and all texels in cache memory and all texels from the neighborhood can be accessed simultaneously in cache memory (using different cache lines with different tags)...Consequently, the relevant texel information [from multiple cache lines, Van Hook lines 15-20] may be retrieved in one clock cycle." (Column 15, line 51 through Column 16, line 20).

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

August 2, 2003

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600